END SEMESTER EXAMINATION MAY-2023

Course Name: - B.Tech **Semester:- IV**

Paper Name: - Computer Organization & Architecture **Paper Code:- TCS-404**

Time - 3 Hrs + 20 minutes per hour extra time for V.I. & examinees with writer. **Max Marks-70**

समय– 3 घण्टे + 20 मिनट प्रति घंटे अतिरिक्त–दृष्टिबाधित एवं सह लेखक परीक्षार्थियों के लिए। अधिकतम अंक–70

Instructions:

- The question paper consists of three sections namely A, B, C. All sections are compulsory.
- Section A- Each question carries 3 mark. All questions are compulsory.
- Section B- Answer any 5 out of 7 given questions in maximum hundred (150) words. Each question carries 7 marks.
- Section C- Answer any 2 out of 3 given questions in maximum five hundred (500) words. Each question carries 10 marks.

निर्देश:

- प्रश्न पत्र में तीन खण्ड अ, ब, व स हैं। सभी खण्ड अनिवार्य हैं।
- खण्ड–अ में प्रत्येक प्रश्न तीन अंक का है। सभी प्रश्न अनिवार्य हैं।
- खण्ड–ब में छः प्रश्नों में से किन्हीं पाँच प्रश्नों के उत्तर अधिकतम 150 शब्दों में दें। प्रत्येक प्रश्न सात अंक का है।
- खण्ड–स में तीन प्रश्नों में से किन्हीं दो प्रश्नों के उत्तर अधिकतम (300) शब्दों में दें। प्रत्येक प्रश्न 10 अंक का है।

Section – A (खण्ड–अ)

Objective Questions (वस्तुनिष्ठ प्रश्न)

1. Answer all the following questions. 5×3 =15

निम्नलिखित सभी प्रश्न अनिवार्य हैं।

i) Which of the following addressing modes does not require any operand in the instruction itself?
   a) Immediate mode
   b) Register mode
   c) Indirect mode
   d) Implicit mode

ii) In which addressing mode is the effective address calculated by adding a constant value to the contents of a register?
   a) Immediate mode
   b) Indexed mode
   c) Indirect mode
   d) Relative mode

iii) Which of the following is true about cache memory?
   a) It is faster than main memory.
   b) It has larger capacity than main memory.
   c) It stores data permanently.
   d) It is located outside the CPU.

iv) Which level of memory hierarchy is typically the smallest and fastest?
   a) Level 1 cache
   b) Level 2 cache
   c) Main memory
   d) Secondary storage

v) Which of the following is a disadvantage of programmed I/O?
   a) It requires a large number of I/O interface circuits

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b) It requires dedicated device controllers for each peripheral device
c) It consumes a significant amount of CPU time for data transfer
d) It provides faster data transfer rates compared to other techniques

Section - B (खण्ड–ब)
Short Answer Questions (लघूत्तरीय प्रश्न)

2. Answer any five of the following questions in maximum 150 words. **5×7=35**
निम्नलिखित में से किन्हीं पाँच प्रश्नों के उत्तर अधिकतम 150 शब्दों में दें।

i. Describe the concept of PC-relative addressing mode and discuss its significance in branch instructions. Compare and contrast direct and indirect addressing modes.
ii. How does the control unit coordinate the operations of the ALU and other components in the data path? What is the purpose of registers in a data path?
iii. Explain the difference between general-purpose registers and special-purpose registers in a CPU. List and briefly describe the commonly used general-purpose registers found in most CPUs.
iv. How does the number and size of CPU registers impact the performance of a computer system? Explain the concept of register transfer and provide an example.
v. What is the purpose of an I/O interface in a computer system? Describe the function of a Universal Serial Bus (USB) interface.
vi. Explain the concept of instruction pipelining. What are the benefits of using pipelining in a processor?
vii. Explain the concept of byte addressing and word addressing in memory organization.

Section - C (खण्ड–स)
Descriptive Questions (विवरणात्मक प्रश्न)

3. Answer any two of the following question in maximum 300 words. **2×10=20**
निम्नलिखित में से किन्हीं दो प्रश्नों के उत्तर अधिकतम 300 शब्दों में दें।

i) **(a)** Explain how the computer buses can be communicate with memory and I/O. Also draw the block diagram for CPU-IOP communication.

(b) Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. Find the number of bits in the TAG, LINE and WORD fields.

ii) **(a)** Discuss the concept of a memory hierarchy and its advantages.

(b) Consider a system with 2 level caches. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

iii) **(a)** Describe the following organizations of cache mapping:
i) Associative Mapping ii) Direct Mapping

(b) Suppose a computer system uses a direct-mapped cache with a cache size of 8 KB and a cache line size of 32 bytes. Calculate the number of cache lines in the cache memory.

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